etitioner's Docket No. MI22-1322

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

pplication of:

Agarwal, Vishnu K.

lication No.:

09/512,149

Group Art No.:

1554

02/23/2000 Examiner: Unknown

Filed: For:

Integrated Circuitry and Method of Forming a Capacitor

Assistant Commissioner for Patents Washington, D.C. 20231

REQUEST FOR CORRECTED FILING RECEIPT

- 1. Attached is a copy of the official filing receipt received from the PTO in the above application for which issuance of a corrected filing receipt is respectfully requested.
- 2. There is an error with respect to the following, which is incorrectly entered.

Error in

Correct data

1. Title

- 2. Integrated Circuitry and Method of Forming a Capacitor
- 3. The correction is not due to any error by applicant and no fee is due.

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SERIAL NUMB 09/512,149	ER	FILING DATE 02/23/2000 RULE _	CLASS C 257		GROUP ART UNIT 2811		ATTORNEY DOCKET NO. MI22-1322		
APPLICANTS Vishnu K Agarwal, Boise, ID; ** CONTINUING DATA **********************************									
85 USC 119 (a-d) conditions M						HEETS TOTAL AWING CLAIR 5 55		MS CLAIMS	
ADDRESS - 021567 TITLE Integrated circuitry and method of forming a capacitor									
RECEIVED	IVED No to charge/credit DEPOSIT ACCOUNT					☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other ☐ Credit			